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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,042	10/15/2001	Hidemi Noguti	2000-315367US	4342

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EXAMINER	
MEEK, JACOB M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/976,042	Applicant(s) NOGUTI, HIDEMI	
	Examiner Jacob Meek	Art Unit 2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8, 14 - 21, 28 - 31* is/are rejected.

7)☒ Claim(s) *9 - 13, 22 - 27, 32 - 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/03,12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. Please confirm spelling of inventor's name on declaration. Signature (Noguchi) does not match typed name (Noguti), and provide correction if necessary.

Specification

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 13 – 38 (see page 23 and 24 of application) been renumbered 12 - 37.

Claim Objections

3. Claim 2 is objected to because of the following informalities:

Limitation of claim 2 from page 19, line 24 – page 20 line 1 states that delayed 2nd signal is sampled by 2nd signal. Figure 1 shows delayed 2nd signal sampled by 1st signal. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1- 3, and 14 - 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al (US-5,473,639).

With regard to claim 1, Lee teaches an out-of-sync detector that detects whether or not two signals are synchronized with each other compromising: a 1st circuit for delaying one of said two signals by a predetermined phase (see Figure 2, 23 and column 3, line 63 column 4, line 5); a second circuit for sampling outputs of 1st circuit in sync with a transition of other of two signals (see figure 2, 24 and column 4, lines 6 – 22); a 3rd circuit for outputting an average value of an output from 2nd circuit (see figure 2, 25, 26, 27, 28 and column 4, lines 28 – 33 where this is interpreted as equivalent); and a 4th circuit for comparing average value with a predetermined threshold value and detecting the presence or absence of out-of-synchronization (see figure 2, 31, 32, 33 and column 4, lines 33 – 45).

With regard to claim 2, Lee teaches an out-of sync detector which receives a 1st signal and a 2nd signal of which the phase and frequency are synchronized of 1st signal and detects whether or not 1st signal is synchronized with 2nd signal (see figure 1 and abstract) compromising: a delay circuit for delaying 2nd signal by a predetermined phase (see Figure 2, 23 and column 3, line 63 column 4, line 5), a sequential logical circuit for sampling 2nd signal delayed by delay circuit, in sync with a falling or rising transition of 1st signal (see objection above) (see figure 2, 24 and column 4, lines 6 – 22 where D flip-flop is a sequential logic circuit); a 3rd circuit for outputting an average value of an output from 2nd circuit (see figure 2, 25, 26, 27, 28 and column 4, lines 28 – 33 where this is interpreted as equivalent); and a 4th circuit for comparing average value with a predetermined threshold value and detecting the presence or absence of out-of-synchronization (see figure 2, 31, 32, 33 and column 4, lines 33 – 45).

With regard to claim 3, Lee teaches an out-of sync detector wherein 2nd signal compromises an oscillation output signal of a signal oscillator (see figure 1, clock signal), signal oscillator receiving a control signal having a value corresponding to a difference in frequency and phase between 1st signal and 2nd signal and varying its oscillation frequency under control signal (see figure 1, VCO, 11 and column 3, lines 20 – 25).

With regard to claim 14, Lee teaches a receiver (see column 1, lines 7 – 9) compromising the elements analyzed in claim 1, and is similarly analyzed.

With regard to claim 15, Lee teaches a receiver (see column 1, lines 7 – 9) compromising: a receiving circuit (see Figure 1, 18); a delay circuit for delaying 2nd signal by a predetermined phase (see Figure 2, 23 and column 3, line 63 column 4, line 5), a sequential logical circuit for sampling 2nd signal delayed by delay circuit, in sync with a falling or rising transition of 1st signal (see objection above) (see figure 2, 24 and column 4, lines 6 – 22 where D flip-flop is a sequential logic circuit); a 3rd circuit for outputting an average value of an output from 2nd circuit (see figure 2, 25, 26, 27, 28 and column 4, lines 28 – 33 where this is interpreted as equivalent); and a 4th circuit for comparing average value with a predetermined threshold value and detecting the presence or absence of out-of-synchronization (see figure 2, 31, 32, 33 and column 4, lines 33 – 45).

With regard to claim 16, Lee teaches a receiver (see column 1, lines 7 – 9) compromising the elements analyzed in claim 3, and is similarly analyzed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US-5,473,639).

With regard to claim 4, Lee teaches an out-of sync detector wherein delay circuit delays 2nd signal by a known phase component (see column 3, lines 63 – 67). Lee is silent with respect to delay being a half pulse width. Lee states in abstract that clock signal is delayed by a fraction of its nominal period. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to utilize ½ pulse width as a delay value.

With regard to claim 17, Lee teaches a receiver (see column 1, lines 7 – 9) compromising the elements analyzed in claim 4, and is similarly analyzed.

6. Claims 5 – 8, 18 – 21, and 28 -31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al ('639) in view of Greeff et al (US-5,719,908).

With regard to claim 5, Lee teaches an out-of sync detector compromising: a delay circuit for delaying a clock from a signal oscillator by a predetermined phase (see Figure 2, 23 and column 3, line 63 column 4, line 5), the oscillation frequency of signal oscillator being varied by a control signal (see figure 1, VCO, 11 and column 3, lines 20 – 25); a flip-flop for sampling a clock delayed by delay circuit, at a falling or rising transition of data signal (see figure 2, 24 and column 4, lines 6 – 22); an average value detector for detecting and outputting an average of an output from flip-flop (see figure 2, 25, 26, 27, 28 and column 4, lines 28 – 33 where this is interpreted as equivalent); and a comparator for comparing average value with a predetermined threshold value and detecting the presence or absence of out-of-synchronization (see figure 2, 31, 32, 33 and column 4, lines 33 – 45). Lee is silent with respect to the issuing of an out-of sync alarm. Greeff teaches a bit synchronization circuit of a similar configuration to Lee's invention, which includes a lock indication output

(see figure 3, 65 where this is interpreted as equivalent functionality). It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a lock indication circuit to provide better monitoring of circuit operation.

With regard to claim 6, Lee teaches an out-of sync detector wherein signal oscillator compromises a VCO (see figure 1, VCO), VCO receiving a control signal having a value corresponding to a difference in frequency and phase from frequency phase comparator (see figure 1, 10, 11) oscillating at an oscillation frequency under control signal (see figure 1, VCO, 11 and column 3, lines 20 – 25), and outputting an oscillation clock, phase frequency comparator receiving received data and clock (see figure 1, 10, clock signal, data signal).

With regard to claim 7, Lee teaches an out-of sync detector wherein delay circuit delays clock by a known phase component (see column 3, lines 63 – 67). Lee is silent with respect to delay being a half pulse width. Lee states in abstract that clock signal is delayed by a fraction of its nominal period. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to utilize ½ pulse width as a delay value.

With regard to claim 8, Lee teaches an out-of sync detector wherein delay circuit delays clock by a known phase component (see column 3, lines 63 – 67). Lee is silent with respect to delay being 90 degrees. Lee states in abstract that clock signal is delayed by a fraction of its nominal period. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to utilize 90 degrees as a delay value.

With regard to claim 18, Lee in view of Greeff teaches a receiver (see column 1, lines 7 – 9) compromising the elements analyzed in claim 5, and is similarly analyzed.

With regard to claim 19 -21, Lee teaches a receiver (see column 1, lines 7 – 9) compromising the elements analyzed in claims 6 - 8, and are similarly analyzed.

With regard to claim 28, Lee in view of Greeff teaches a receiver (see column 1, lines 7 – 9, and column 2, lines 62 – 65 where this is interpreted as a recovered optical OC-12 signal) compromising the elements analyzed in claim 5, and is similarly analyzed.

With regard to claim 19 -21, Lee teaches a receiver (see column 1, lines 7 – 9) compromising the elements analyzed in claims 6 - 8, and are similarly analyzed.

Allowable Subject Matter

7. Claims 9 – 13, 22 – 27, and 32 – 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Cited Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dunn (US-4,069,462), Baumert (US-5,406,592), Miyashita (US-5,889,828), Tan (US-6,211,742), and Dietrich (US-6,785,354) disclose PLL's with lock detection circuitry. Byrn (US-6,011,412) discloses a device for the adjustment of phase / frequency relationships. Kallman (US-5,694,440) discloses a synchronization lock detector.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM

JAY K. PATEL
SUPERVISORY PATENT EXAMINER